NEC

MOS INTEGRATED CIRCUIT

μPD17P149

SMALL, GENERAL-PURPOSE 4 BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P149 is a one-time PROM version of the μPD17149. It uses a one-time PROM, which can be written just once, instead of internal masked ROM of the μPD17149.

Since a user program can be written into the PROM, this microcontroller is suited for program evaluation and low-volume production of the μPD17145, μPD17147, μPD17149, or for program evaluation of the μPD17145(A), μPD17147(A), μPD17149(A), μPD17145(A1), μPD17147(A1), and μPD17149(A1). ★

The following user's manual completely describes the functions of the μPD17P149. Be sure to read it before designing an application system.

μPD17145 Sub-Series User's Manual: U10261E

FEATURES

- 17K architecture : General registers, 16-bit instructions
- Pin compatible with the μPD17149 (except for PROM programming function)
- Internal one-time PROM : 8K bytes (4096 × 16 bits)
- Supply voltage : V_{DD} = 2.7 to 5.5 V (when operating at the range between 400 kHz and 2 MHz with ceramic oscillation)
  V_{DD} = 4.5 to 5.5 V (when operating at the range between 400 kHz and 8 MHz with ceramic oscillation)

ORDERING INFORMATION

Part number	Package
μPD17P149CT	28-pin plastic shrink DIP (400 mil)
μPD17P149GT	28-pin plastic SOP (375 mil)

In the program memory write/verify mode, the voltage used for programming is applied to pin No. 23, P0F0/$\overline{\text{RLS}}$/V_{PP}. If a voltage of V_{DD} plus 0.3 V or more is applied to this pin in the normal operation mode, the microcontroller may crash. Design the circuit so that a voltage of this magnitude is never applied to the pin.

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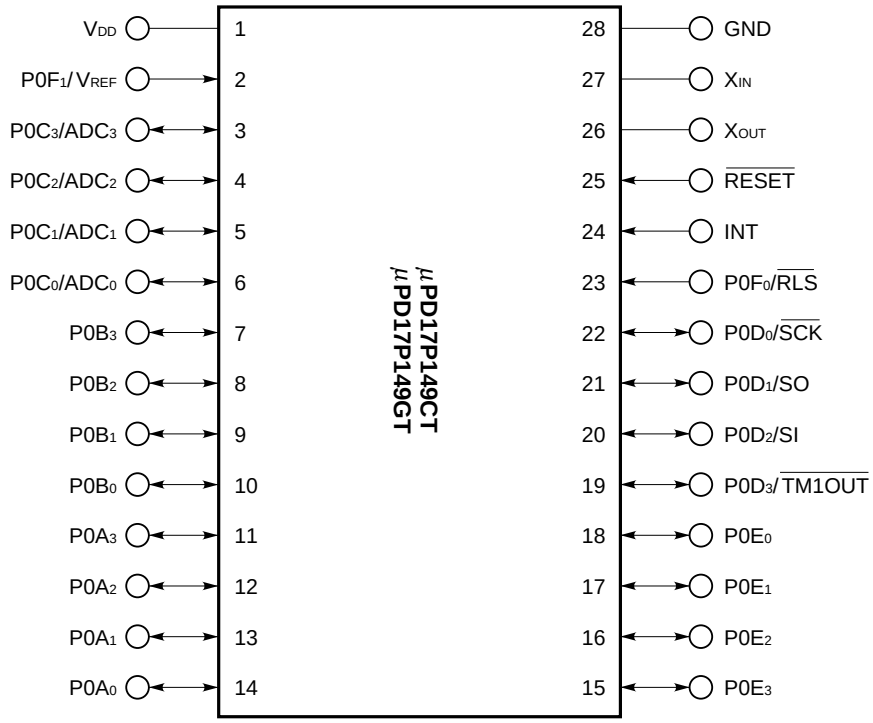
Date Published May 1996 P
Printed in Japan

The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)

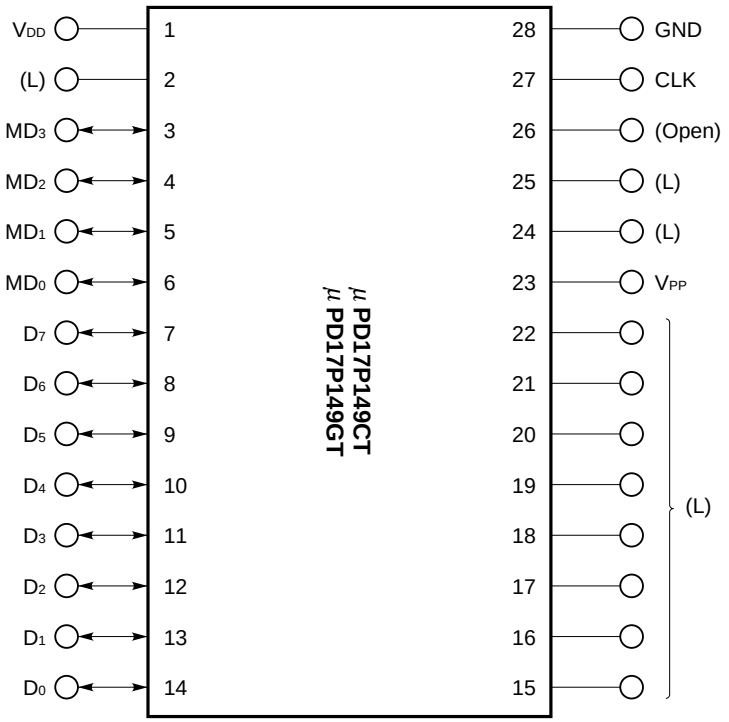
(1) Normal operation mode



ADC_0 - ADC_3	:	Analog input
GND	:	Ground
INT	:	External interrupt input
$P0A_0$ - $P0A_3$	:	Port 0A
$P0B_0$ - $P0B_3$	:	Port 0B
$P0C_0$ - $P0C_3$	:	Port 0C
$P0D_0$ - $P0D_3$	:	Port 0D
$P0E_0$ - $P0E_3$	:	Port 0E
$P0F_0$ and $P0F_1$	:	Port 0F

$\overline{RESET}$	:	Reset input
$\overline{RLS}$	:	Standby release signal input
$\overline{SCK}$	:	Serial clock input/output
SI	:	Serial data input
SO	:	Serial data output
$\overline{TM1OUT}$	:	Timer 1 carry output
V_{DD}	:	Power supply
V_{REF}	:	Reference voltage for the A/D converter
X_{IN}, X_{OUT}	:	System clock oscillation

(2) Program memory write/verify mode



CLK : Input clock for address update

D_0 - D_7 : Data

GND : Ground

MD_0 - MD_3 : Operating mode selection

V_{DD} : Power supply

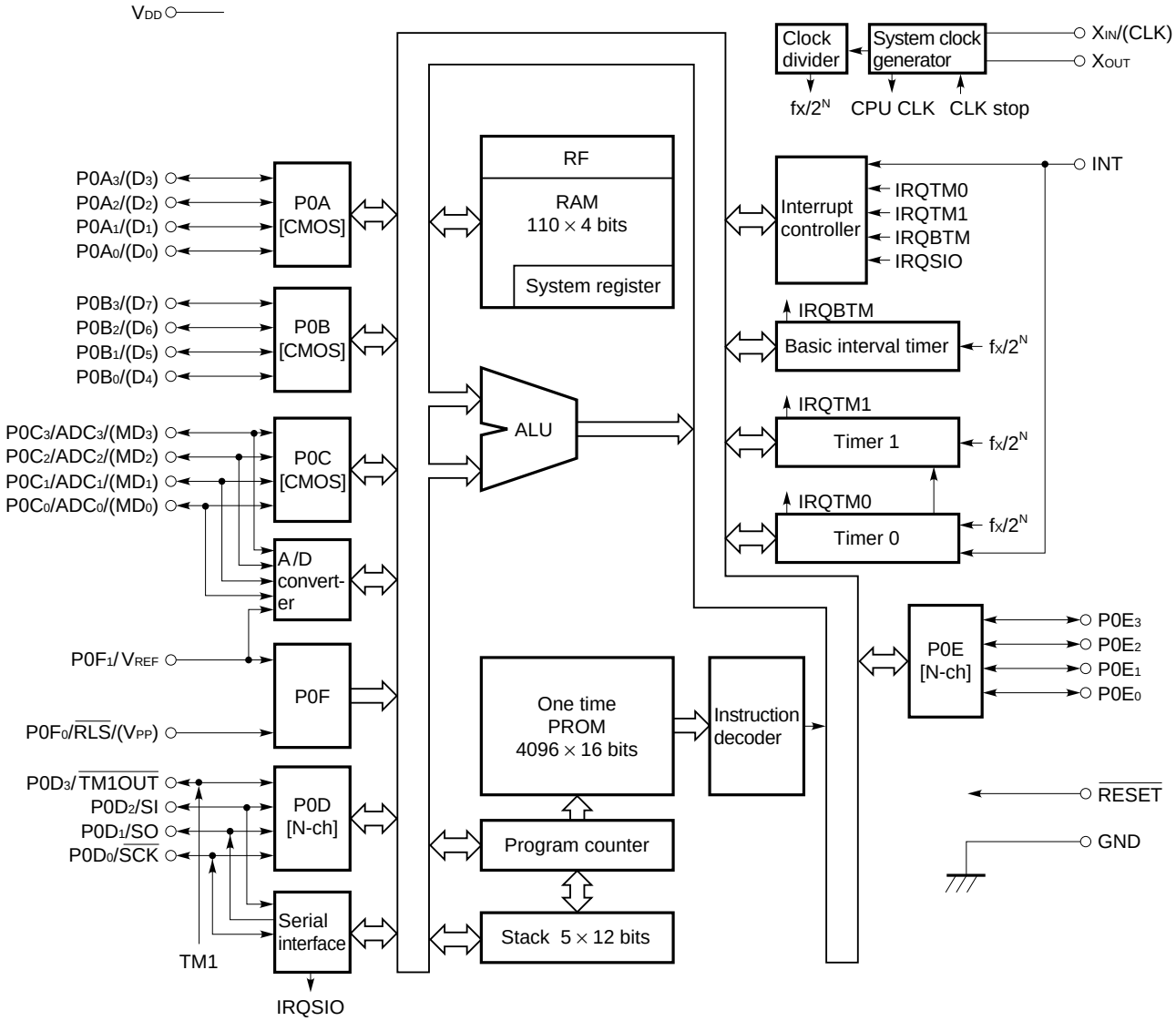
V_{PP} : Programming power supply

Caution Symbols in parentheses denote processing for pins not used in the program memory write/verify mode.

L : Connect these pins separately to the GND pin through pull-down resistors.

Open : Nothing should be connected on these pins.

BLOCK DIAGRAM



Remark ( ) : PROM programming mode

The terms CMOS and N-ch in brackets indicate the output form of the port.

CMOS : CMOS push-pull output

N-ch : N-channel open-drain output

CONTENTS

1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

Pin No.	Symbol	Function	Output	Upon reset
1	V_{DD}	Power supply	–	–

2	$P0F_1/V_{REF}$	Port 0F. The reference voltage is supplied to the A/D converter through this pin.
		• $P0F_1$
		  • Bit 1 of 2-bit input port P0F
		• V_{REF}
		  • Reference voltage input for the A/D converter
			Input	Input ($P0F_1$)

3 - 6	$P0C_3/ADC_3$ - $P0C_0/ADC_0$	Port 0C. Analog voltage is supplied to the A/D converter through these pins.
		• $P0C_3$ - $P0C_0$
		  • 4-bit input/output port
		  • Input/output setting allowed in units of 1 bit
		• ADC_3 - ADC_0
		  • Analog input for the A/D converter
			CMOS push-pull	Input (P0C)

7 8 9 10	$P0B_3$ $P0B_2$ $P0B_1$ $P0B_0$	Port 0B • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	CMOS push-pull	Input
11 12 13 14	$P0A_3$ $P0A_2$ $P0A_1$ $P0A_0$	Port 0A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	CMOS push-pull	Input
15 16 17 18	$P0E_3$ $P0E_2$ $P0E_1$ $P0E_0$	Port 0E • Withstand voltage is V_{DD} (Max.). • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	N-ch open drain	Input

Pin No.	Symbol	Function	Output	Upon reset

19	$P0D_3/\overline{TM1OUT}$	Pin for port 0D, timer 1 output, serial data input, serial data output, and serial clock input/output
		• Pull-up resistor incorporation specified by program bit by bit
		  • Withstand voltage is V_{DD} (Max.).
		• $P0D_3$ - $P0D_0$
		  • 4-bit input/output port
		  • Input/output setting allowed bit by bit
		• $\overline{TM1OUT}$
		  • Timer 1 output
			N-ch open drain	Input (P0D)

20	$P0D_2$/SI	• SI • Serial data input		
21	$P0D_1$/SO	• SO • Serial data output		
22	$P0D_0/\overline{SCK}$	• $\overline{SCK}$ • Serial clock input/output		

23	$P0F_0/\overline{RLS}$	Pin for port 0F and input for standby mode release signal
		• $P0F_0$
		  • Bit 0 of 2-bit input port P0F
		• $\overline{RLS}$
		  • Input for standby mode release signal
			Input	Input ($P0F_0$)

24	INT	Input for an external interrupt request signal and standby mode release signal.	Input	Input
25	$\overline{RESET}$	System reset input pin	Input	Input
26 27	X_{OUT} X_{IN}	For system clock oscillation The ceramic resonator is connected between X_{IN} and X_{OUT}.	–	–
28	GND	Ground	–	–

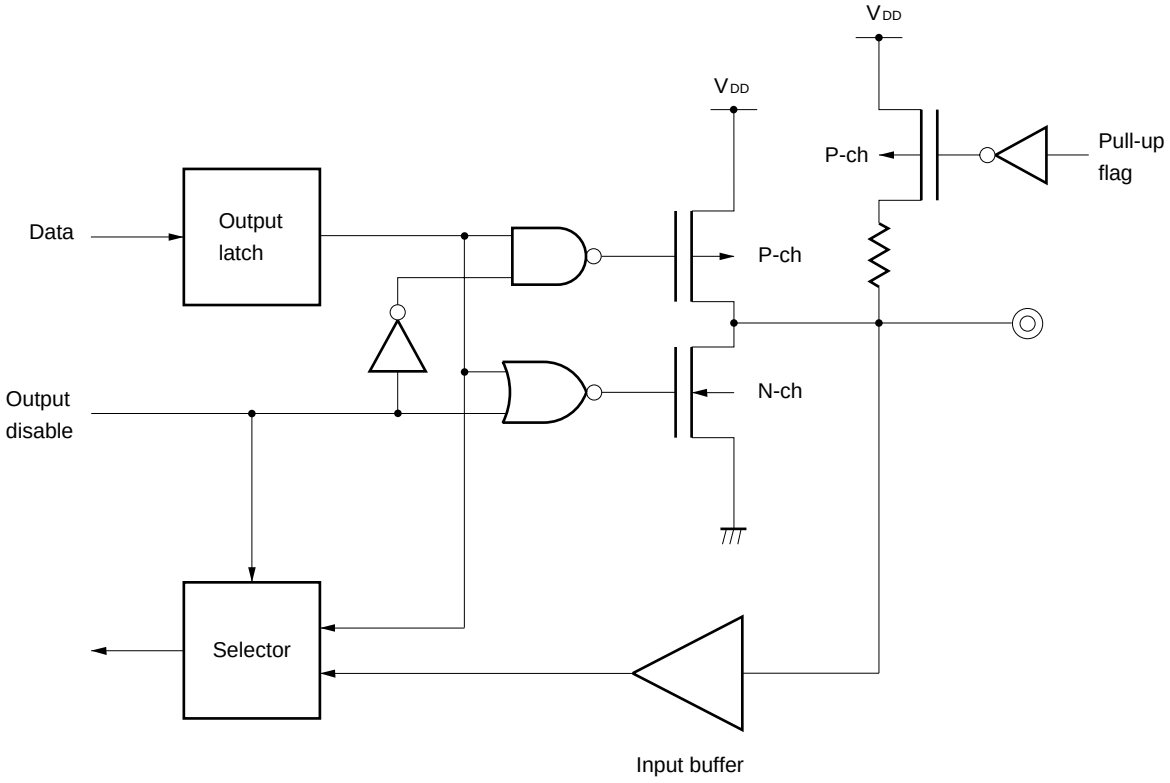
1.2 PROGRAM MEMORY WRITE/VERIFY MODE

Pin No.	Pin name	Function	Input/output
1	V_{DD}	Power supply pin. +6 V is applied to this pin when writing to program memory or verifying its contents.	–
3 to 6	MD_3 to MD_0	Input pins that select an operation mode when writing to program memory or verifying its contents	Input
7 to 14	D_7 to D_0	Input/output pins for 8-bit data used when writing to program memory or verifying its contents	Input/output
23	V_{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.	–
27	CLK	Input pin for address update clocks used when writing to program memory or verifying its contents	Input
28	GND	Ground	–

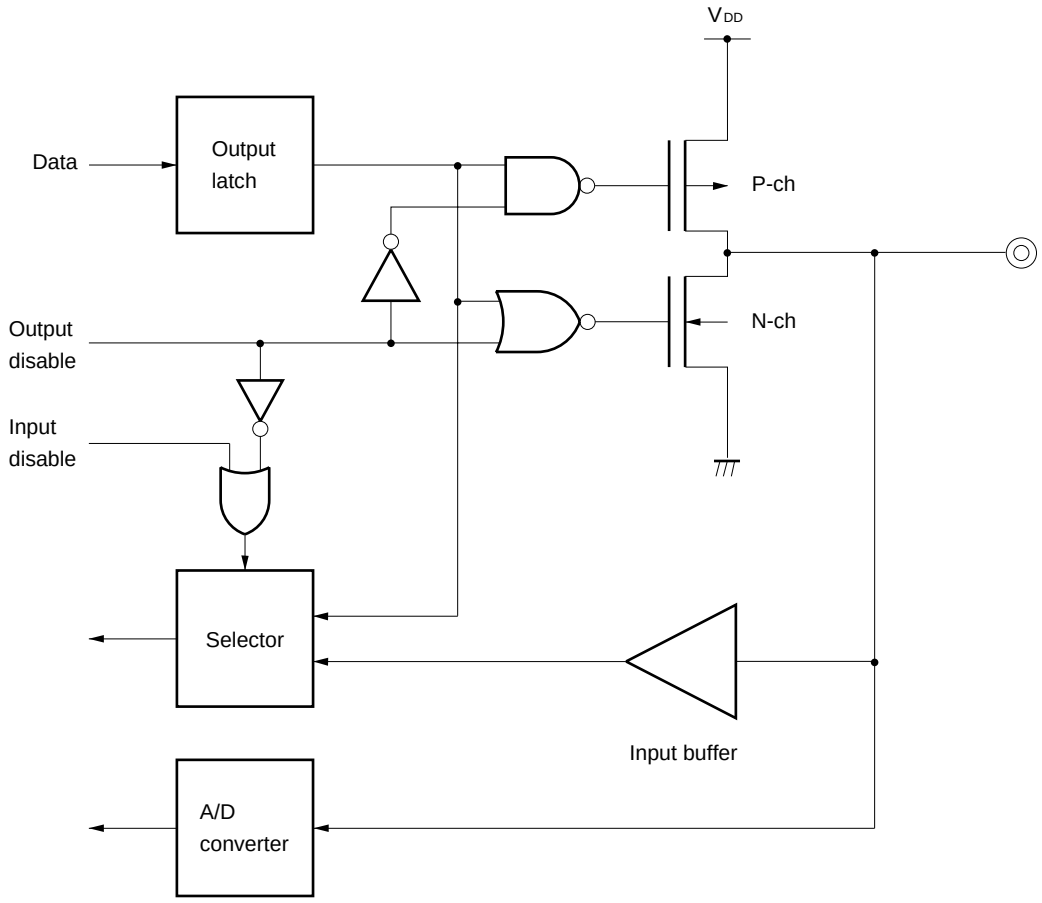
1.3 EQUIVALENT INPUT/OUTPUT CIRCUITS

Below are simplified diagrams of the input/output circuits for each pin.

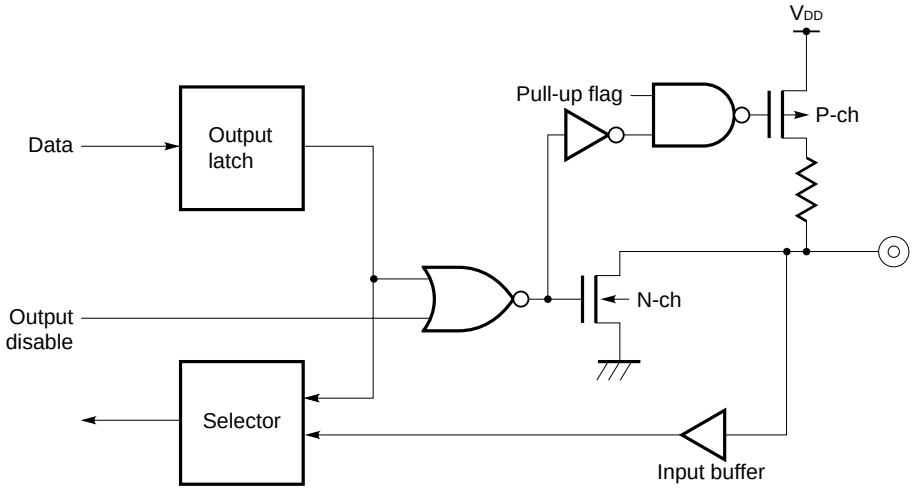
(1) $P0A_0$ - $P0A_3$, $P0B_0$ - $P0B_3$



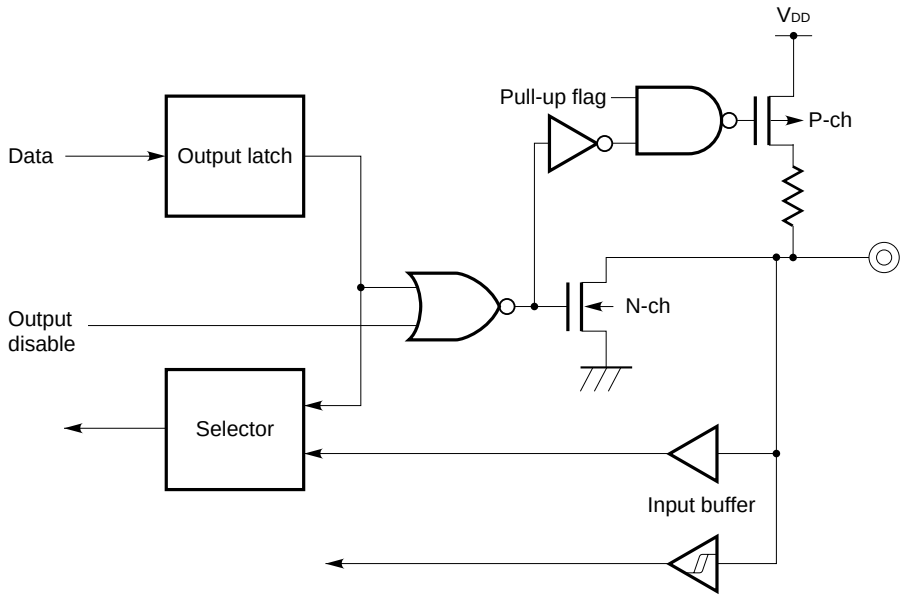
(2) P0C0/ADC0 - P0C3/ADC3



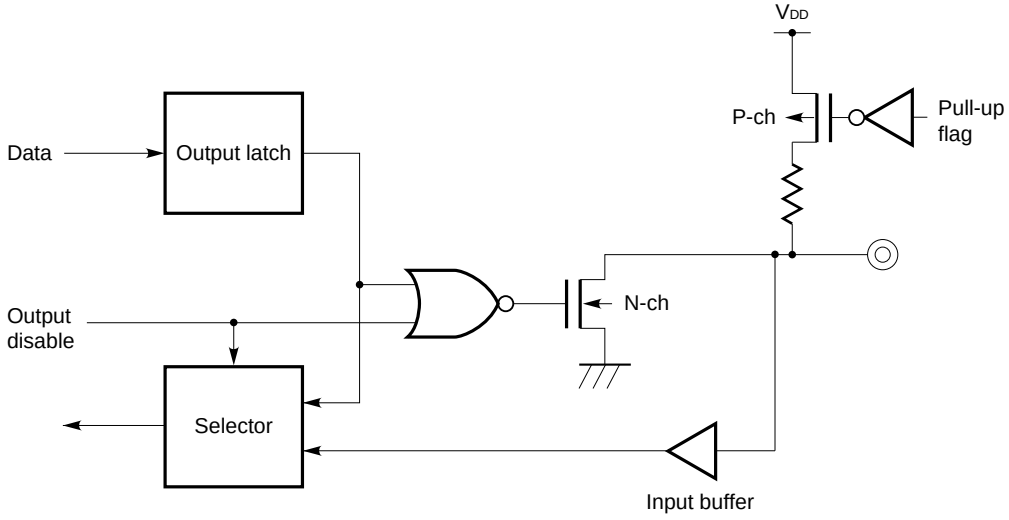
(3) P0D3/$\overline{\text{TM1OUT}}$, P0D1/SO



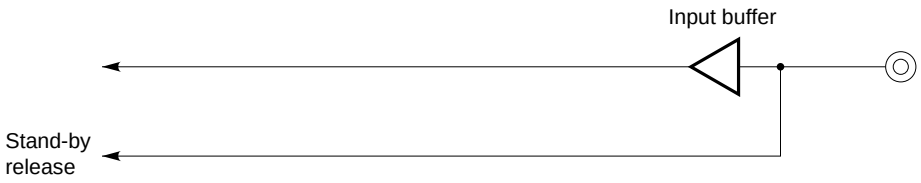
(4) P0D2/SI, P0D0/$\overline{\text{SCK}}$



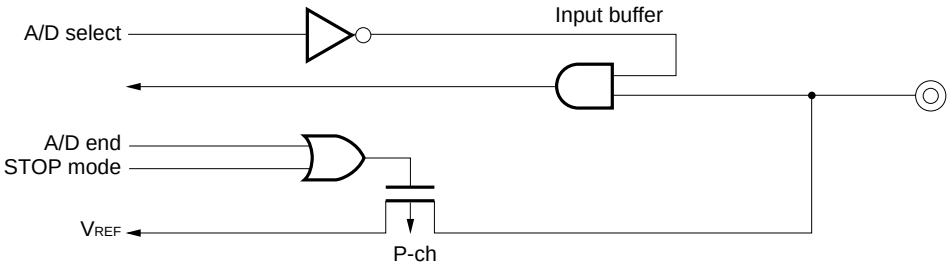
(5) P0E0 - P0E3



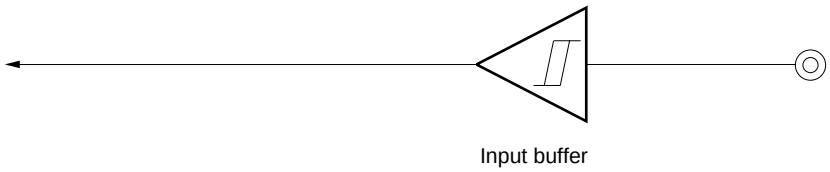
(6) P0F0/$\overline{\text{RLS}}$



(7) P0F1/VREF



(8) $\overline{\text{RESET}}$, INT



1.4 HANDLING UNUSED PINS

Connect unused pins at the normal operation mode as follows:

Table 1-1 Handling Unused Pins ★

Pin			Conditions and handling	
			Internal	External
Port	Input mode	P0A, P0B, P0D, P0E	Pull-up resistors that can be specified with the software are incorporated.	Leave open.
		P0C	—	Connect to V_{DD} or ground through resistors for each pin.**Note 1**
		$P0F_1$	—	Connect directly to V_{DD} or ground.
		$P0F_0$**Note 2**	—	Connect directly to ground.
	Output mode	P0A, P0B, P0C (CMOS ports)	—	Leave open.
		P0D (N-ch open-drain port)	Outputs low level.	
		P0E (N-ch open-drain port)	Outputs low level without pull-up resistors that can be specified with the software.	
			Outputs low level with pull-up resistors that can be specified with the software.	
External interrupt (INT)			—	Connect directly to V_{DD} or ground.

Notes 1. When a pin is pulled up to V_{DD} (connected to V_{DD} through a resistor) or pulled down to ground (connected to ground through a resistor) outside the chip, take the driving capacity and maximum current consumption of a port into consideration. When using high-resistance pull-up or pull-down resistors, apply appropriate countermeasures to ensure that noise is not attracted by the resistors. Although the optimum pull-up or pull-down resistor varies with the application circuit, in general, a resistor of 10 to 100 kilohms is suitable.

2. Since the $P0F_0/\overline{RLS}$ pin is also used as the V_{PP} pin for writing and verifying the program memory, connect directly to ground when the pin is not used.

Caution To fix the I/O mode, pull-up resistors that can be specified with the software, and output level of a pin, it is recommended that they should be specified repeatedly within a loop in a program.

1.5 NOTES ON USE OF THE $\overline{\text{RESET}}$ AND P0F$_0$/$\overline{\text{RLS}}$ PINS (ONLY AT THE NORMAL OPERATION MODE)

The $\overline{\text{RESET}}$ pin can be used as the test mode selection pin for testing the internal operation of the μPD17P149 (IC test), besides the usage shown in **Section 1.1**.

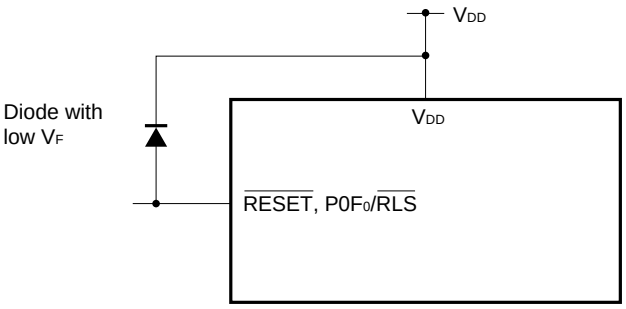
The P0F$_0$/$\overline{\text{RLS}}$ pin can be used as the V_{PP} pin in the program memory write/verify mode.

Applying a voltage exceeding V_{DD} to the $\overline{\text{RESET}}$ or P0F$_0$/$\overline{\text{RLS}}$ pin causes the μPD17P149 to enter the test mode or program memory write/verify mode. When noise exceeding V_{DD} comes in during normal operation, the device may not operate normally.

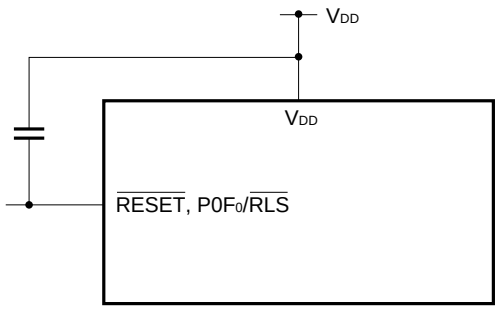
For example, if the wiring from the $\overline{\text{RESET}}$ or P0F$_0$/$\overline{\text{RLS}}$ pin is too long, noise may be induced on the wiring, causing this mode switching.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- **Connect a diode with low V_F between the pin and V_{DD}.**



- **Connect a capacitor between the pin and V_{DD}.**



2. DIFFERENCES BETWEEN THE μPD17145, μPD17147, μPD17149, AND μPD17P149

The μPD17P149 is a one-time PROM version of the μPD17149, in which the internal mask ROM is replaced with a one-time PROM.

Table 2-1 lists the differences between the μPD17145, μPD17147, μPD17149, and μPD17P149.

The μPD17P149 has the same CPU functions and internal peripheral hardwares as those of μPD17145, μPD17147, and μPD17149 except for its program memory, program size, address register size, and mask option.

Part of electrical characteristics is also different between those products. For details of the electrical characteristics, refer to the data sheet of each product.

Table 2-1 Differences between the μPD17145, μPD17147, μPD17149, and μPD17P149

Item	μPD17145	μPD17147	μPD17149	μPD17P149
Program memory (ROM)	Masked ROM			One-time PROM
	1024 × 16 bits (0000H-03FFH)	2048 × 16 bits (0000H-07FFH)	4096 × 16 bits (0000H-0FFFH)	
Program counter (PC)	10 bits	11 bits	12 bits	
Address register (AR)				
Address stack register				
Pull-up resistors of P0F, $\overline{\text{RESET}}$, and INT pins	Mask option			Not provided
Internal POC circuit	Mask option			Not provided
V_{PP} pin and operating mode selection pin	Not provided			Provided
Quality grade	• Standard μPD17145 • Special μPD17145 (A) μPD17145 (A1)	• Standard μPD17147 • Special μPD17147 (A) μPD17147 (A1)	• Standard μPD17149 • Special μPD17147 (A) μPD17147 (A1)	Standard
Electrical characteristics	Partially differs between these products. Refer to the data sheet of each product for details.			

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Caution Although a PROM product is highly compatible with a mask ROM product in respect of functions, they differ in internal ROM circuits and part of electrical characteristics. Before changing the PROM product to the mask ROM product in an application system, evaluate the system carefully using the mask ROM product.

3. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P149's internal program memory consists of a 4096 × 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in Table 3-1. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Caution The P0F0/$\overline{\text{RLS}}$/V_{PP} pin is used as the V_{PP} pin when writing to program memory or verifying its contents. If an voltage equal to or more than V_{DD} + 0.3 V is applied to the P0F0/$\overline{\text{RLS}}$ pin in normal operation mode, the microcontroller may cause a system crash. Protect the pins from high voltages.

Table 3-1 Pins Used When Writing to Program Memory or Verifying Its Contents

Pin	Function
V_{PP}	Pin for applying programming supply voltage. Voltage (+12.5 V) is applied to this pin.
V_{DD}	Positive power supply pin. +6 V is applied to this pin.
CLK	Input pin for address update clocks. Input of four pulses to this pin updates the address of the program memory.
MD_0 - MD_3	Input pins that select an operation mode
D_0 - D_7	Input/output pins for 8-bit data

3.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{\text{RESET}}$ = 0 V), the μPD17P149 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. The X_{OUT} pin must be left open. Connect each pin not listed in Table 3-1 (including the $\overline{\text{RESET}}$ pin) to ground through a resistor.

Table 3-2 Specification of Operating Modes

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

Remark ×: Don't care. L (low) or H (high)

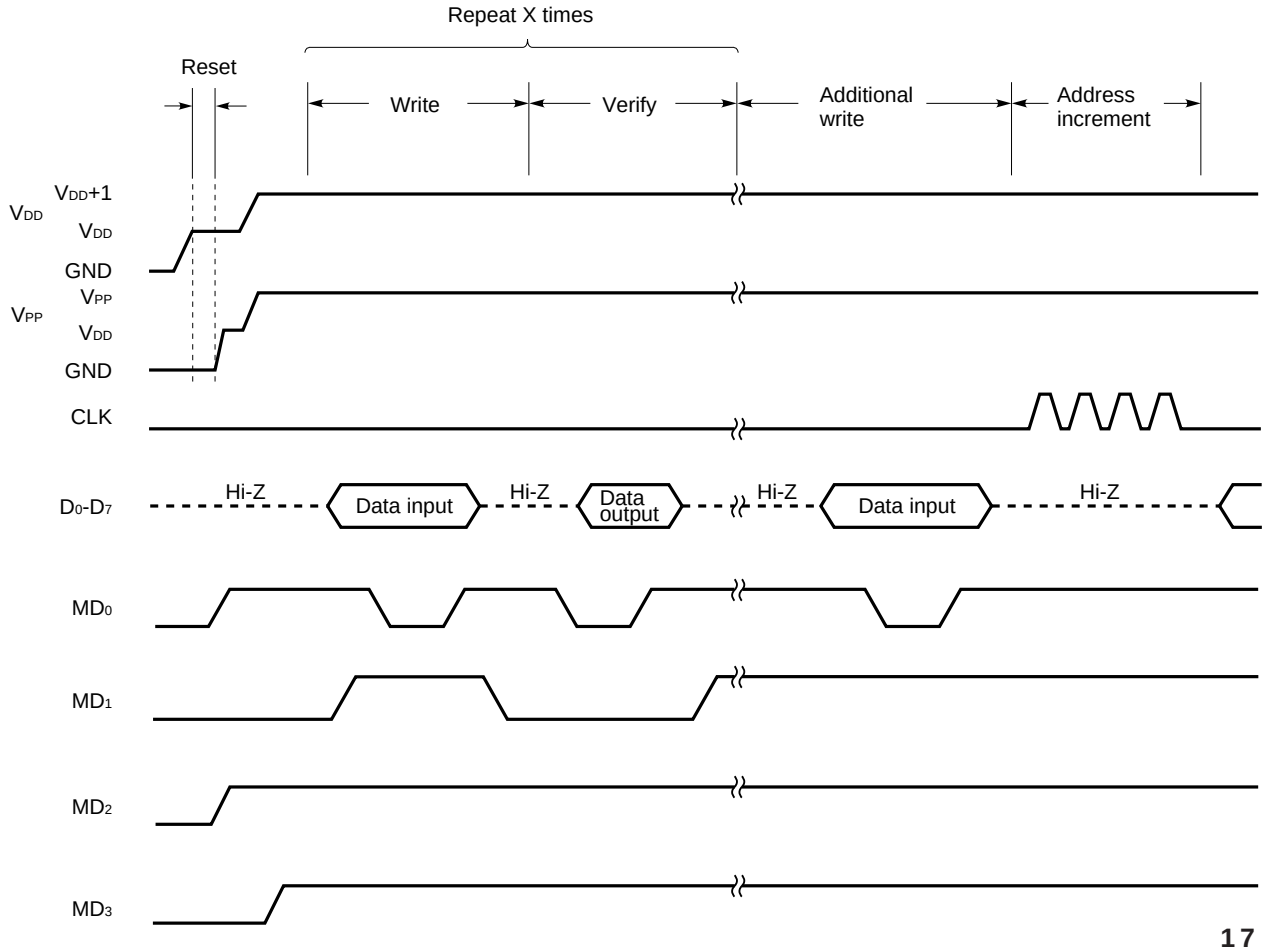
3.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below.

(1) Connect all unused pins to GND through resistors (the X_{OUT} pin is left open). Apply a low-level signal to the CLK pin.
(2) Apply 5 V to V_{DD} and apply a low-level signal to the V_{PP} pin.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1-ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for X (number of repetitions of steps (7) to (9)) × 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the CLK pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

A timing chart for program memory writing steps (2) to (12) is shown in Fig. 3-1.

Fig. 3-1 Timing Chart for Program Memory Writing Steps

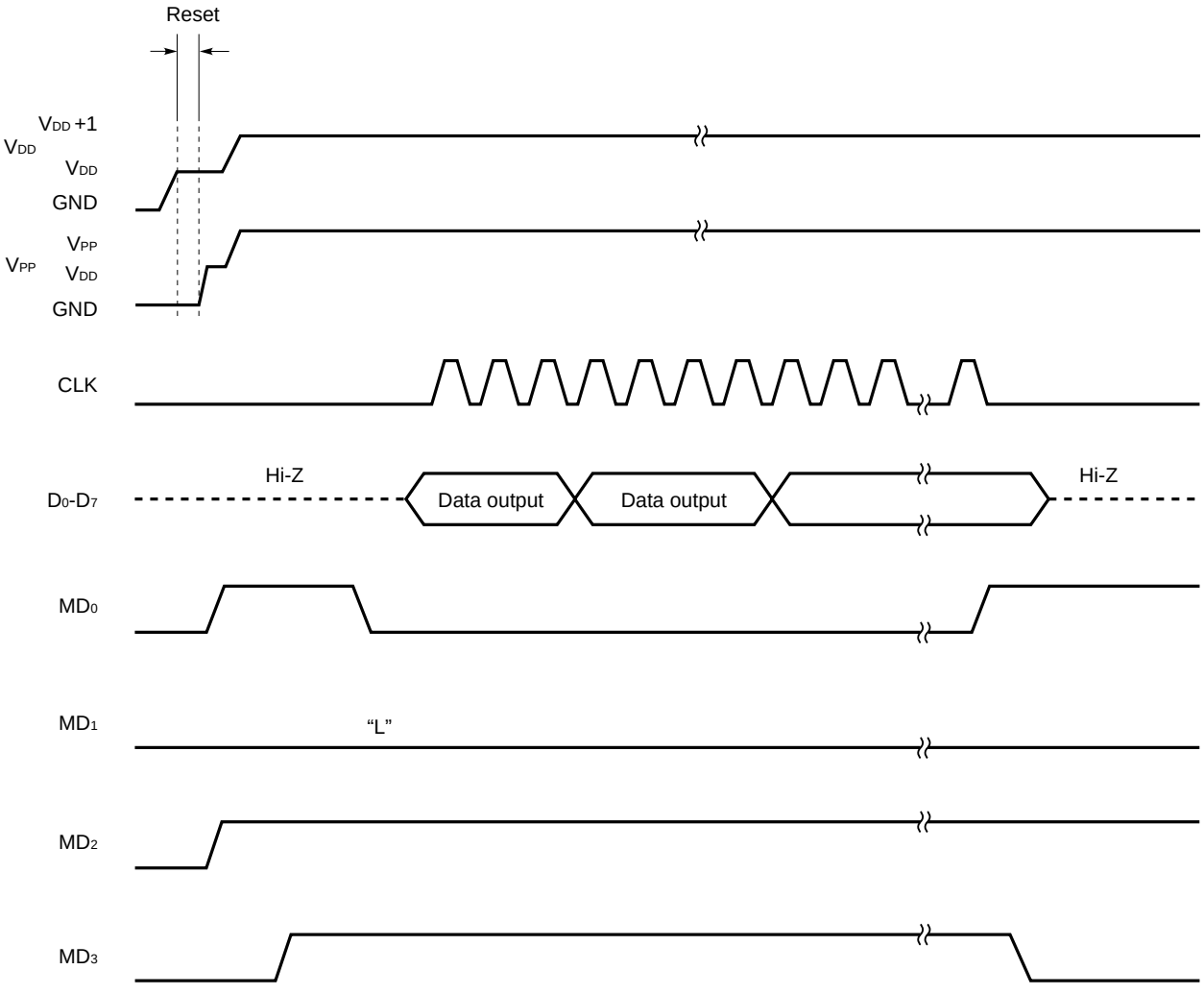


3.3 READING PROGRAM MEMORY

(1) Connect all unused pins to GND through resistors (the X_{OUT} pin is left open). Apply a low-level signal to the CLK pin.
(2) Apply 5 V to V_{DD} and apply a low-level signal to the V_{PP} pin.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for every four input clock pulses on the CLK.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

A timing chart for program memory reading steps (2) to (9) is shown below.

★ **Fig. 3-2 Timing Chart for Program Memory Reading Steps**



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
PROM supply voltage	V_{PP}			–0.3 to +13.5	V
A/D converter reference voltage	V_{REF}			–0.3 to V_{DD} + 0.3	V
Input voltage	V_I	P0A, P0B, P0C, P0D, P0E, P0F, INT, $\overline{RESET}$, and X_{IN}		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}**Note**	Each of P0A, P0B, and P0C pins	Peak value	–15	mA
			rms	–7.5	mA
		Total of P0A, P0B, and P0C pins	Peak value	–30	mA
			rms	–15	mA
Low-level output current	I_{OL}**Note**	Each of P0A, P0B, and P0C	Peak value	15	mA
			rms	7.5	mA
		Each of P0D and P0E	Peak value	30	mA
			rms	15	mA
		Total of P0A, P0B, P0C, P0D, and P0E pins	Peak value	100	mA
			rms	50	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C
Allowable dissipation	P_d	T_A = 85 °C	28-pin plastic shrink DIP	140	mW
			28-pin plastic SOP	85	mW

Note Calculate a root-mean-square value as follows: [rms value] = [peak value] × $\sqrt{\text{duty}}$.

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

RECOMMENDED POWER VOLTAGE RANGE (T_A = –40 to +85 °C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	CPU (except A/D converter)	f_X = 400 kHz to 2 MHz	2.7		5.5	V
			f_X = 400 kHz to 4 MHz	3.6		5.5	V
			f_X = 400 kHz to 8 MHz	4.5		5.5	V
		A/D converter	Absolute accuracy: ±1.5 LSB, 2.5 V ≤ V_{REF} ≤ V_{DD}	4.0		5.5	V

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = –40 to +85 °C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	P0A, P0B, P0C, P0D, P0E, and P0F		0.7V_{DD}		V_{DD}	V
	V_{IH2}	RESET, SCK, SI, and INT		0.8V_{DD}		V_{DD}	V
	V_{IH3}	X_{IN}		V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P0A, P0B, P0C, P0D, P0E, and P0F		0		0.3V_{DD}	V
	V_{IL2}	RESET, SCK, SI, and INT		0		0.2V_{DD}	V
	V_{IL3}	X_{IN}		0		0.4	V
High-level output voltage	V_{OH}	P0A, P0B, and P0C	4.5 - V_{DD} - 5.5 I_{OH} = –1.0 mA	V_{DD} – 0.3			V
			2.7 - V_{DD} < 4.5 I_{OH} = –0.5 mA	V_{DD} – 0.3			V
Low-level output voltage	V_{OL1}	P0A, P0B, P0C, P0D, and P0E	4.5 - V_{DD} - 5.5 I_{OL} = 1.0 mA			0.3	V
			2.7 - V_{DD} < 4.5 I_{OL} = 0.5 mA			0.3	V
	V_{OL2}	P0D and P0E	4.5 - V_{DD} - 5.5			1.0	V
		I_{OL} = 15 mA	2.7 - V_{DD} < 4.5			2.0	V
High-level input leakage current	I_{LIH}	P0A, P0B, P0C, P0D, P0E, P0F, RESET, and INT V_{IN} = V_{DD}				3	μA
Low-level input leakage current	I_{LIL}	P0A, P0B, P0C, P0D, P0E, P0F, RESET, and INT V_{IN} = 0 V				–3	μA
High-level output leakage current	I_{LOH}	P0A, P0B, P0C, P0D, and P0E V_{OUT} = V_{DD}				3	μA
Low-level output leakage current	I_{LOL}	P0A, P0B, P0C, P0D, and P0E V_{OUT} = 0 V				–3	μA
Built-in pull-up resistance**Note 1**	R_{PULL}	P0A, P0B, and P0E		50	100	200	kΩ
		P0D		3	10	30	kΩ
Power supply current**Note 2**	I_{DD1}	Normal operation mode	f_X = 8.0 MHz, V_{DD} = 5 V ±10%		5.5	8.0	mA
			f_X = 4.0 MHz, V_{DD} = 5 V ±10%		3.3	5.5	mA
			f_X = 2.0 MHz, V_{DD} = 3 V ±10%		1.0	2.5	mA
			f_X = 400 kHz, V_{DD} = 5 V ±10%		2.0	4.7	mA
			f_X = 400 kHz, V_{DD} = 3 V ±10%		0.7	2.4	mA
	I_{DD2}	HALT mode	f_X = 8.0 MHz, V_{DD} = 5 V ±10%		3.5	5.0	mA
			f_X = 4.0 MHz, V_{DD} = 5 V ±10%		2.7	4.1	mA
			f_X = 2.0 MHz, V_{DD} = 3 V ±10%		0.8	2.0	mA
					1.8	3.8	mA
					0.6	2.2	mA
	I_{DD3}	STOP mode			12	50	μA
					10	45	μA

Notes 1. Pull-up resistors are not incorporated for the P0F, RESET, and INT pins.

2. This current excludes the current which flows through the A/D converter and built-in pull-up resistors.

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